Data Sheet

VT1617
Vinyl Eight-TRAC AC'97 Codec

Revision 1.2
March 3, 2005

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

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1.0	1/14/03	First external release	EY
1.1	5/20/04	Updated recommended operating conditions table and DC characteristics table	EY
1.2	3/2/05	Updated cover page Updated product features Updated overview Updated table 2 pin description for XTL_IN signal Removed PLL setting register (index 74h) Added lead free mechanical specifications	JM

TABLE OF CONTENTS

REVISION HISTORY I
TABLE OF CONTENTS II
LIST OF FIGURES III
LIST OF TABLES IV
PRODUCT FEATURES 1
OVERVIEW 3
PINOUTS 4
- PIN DIAGRAM 4
- PIN LIST 5
- PIN DESCRIPTIONS 6

REGISTERS 8
- REGISTER OVERVIEW 8
- REGISTER DESCRIPTIONS 10

ELECTRICAL SPECIFICATIONS 40
- ABSOLUTE MAXIMUM RATINGS 40
- RECOMMENDED OPERATING CONDITIONS 40
- DC SPECIFICATIONS 40

PACKAGE MECHANICAL SPECIFICATIONS 41

LIST OF FIGURES

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM 3
FIGURE 2. VT1617 PIN DIAGRAM (TOP VIEW) 4
FIGURE 3. MECHANICAL SPECIFICATION – 48-PIN LQFP 41
FIGURE 4. MECHANICAL SPECIFICATION FOR LEAD FREE – 48-PIN LQFP 42

LIST OF TABLES

TABLE 1. PIN LIST (ALPHABETICAL ORDER) 5
TABLE 2. PIN DESCRIPTIONS 6
TABLE 3. REGISTER MAP 9
TABLE 4. STEREO AND MONO OUTPUT ATTENUATION 12
TABLE 5. PROGRAMMABLE MIXER INPUT GAIN LEVELS 17
TABLE 6. MIXER TABLE 20
TABLE 7. 3D DEPTH CONTROL 21
TABLE 8. MULTIPLE CODE MODE STATUS BITS 24

VT1617

Vinyl Eight-TRAC AC'97 Codec

AC'97 2.3 Compliant,
with 96KHz S/PDIF output

PRODUCT FEATURES

- **AC'97 V2.3 Audio Codec**
  - Fully compliant with AC97 Revision 2.3
- **High Audio Quality**
  - Supports sampling rates up to 96KHz
  - Independent 20-bit ADC and 20-bit DAC
  - Top Audio Fidelity ~95dB
  - Built-in Hi-Quality Headphone Amplifier
  - Built-in 1HZ resolution VSR converter
- **Various Output Format**
  - Supports 8ch outputs
  - 96KHz analog output
  - DualMAX™ Hardware Downmix
  - Center and LFE channel swapping
  - Alternative Line-Level outputs at surround outputs
  - 96KHz I2S Digital Output and S/PDIF Digital Output
  - Features Analog input to S/PDIF output
- **Added-on Functions**
  - Dual microphones supporting Karaoke with mixing
  - Microphone sensitivity Enhancement
  - SCMS Mode Supported
  - Integrate Power ON/OFF De-pop circuit
- **Extension Control**
  - 4-bit 3D depth control
  - Supports EAPD control
  - Supports GPIO pins control
  - Selectable clock sources

- **Software features**
  - Built-in Smart 5.1™
  - Immerzio™ 3D Supports EAX1.0, EAX2.0, A3D™1.X, I3DL2, etc…
  - Fancy and Friendly Audio Deck
- **Power**
  - Low power consumption mode
  - 3.3V or 5V analog, 3.3V digital power supply
- **Package**
  - 48-Pin LQFP Package

OVERVIEW

The VT1617 is a high-performance audio codec that complies with the AC '97 revision 2.3. It integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. This chip supports 96KHz sampling rates, high-quality 96KHz S/PDIF output, and stereo digital audio playback.

The 20bit, VT1617 implements stereo recording and white noise removal to ensure the best quality of recording. It features 8-channel hardware-expansion for flexible 7.1-channel applications. It also contains a hardware down-mixing feature that allows the end users enjoy 6-channel audio with 2-channel or 4-channel speakers. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. The VT1617 has a built-in high-quality headphone amplifier for cost saving. This codec is designed with aggressive power management to achieve low power consumption; when used with a 3.3V analog supply, the power consumption is further reduced.

The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, this audio codec is also suitable for any PC based home theater systems at competitive prices.

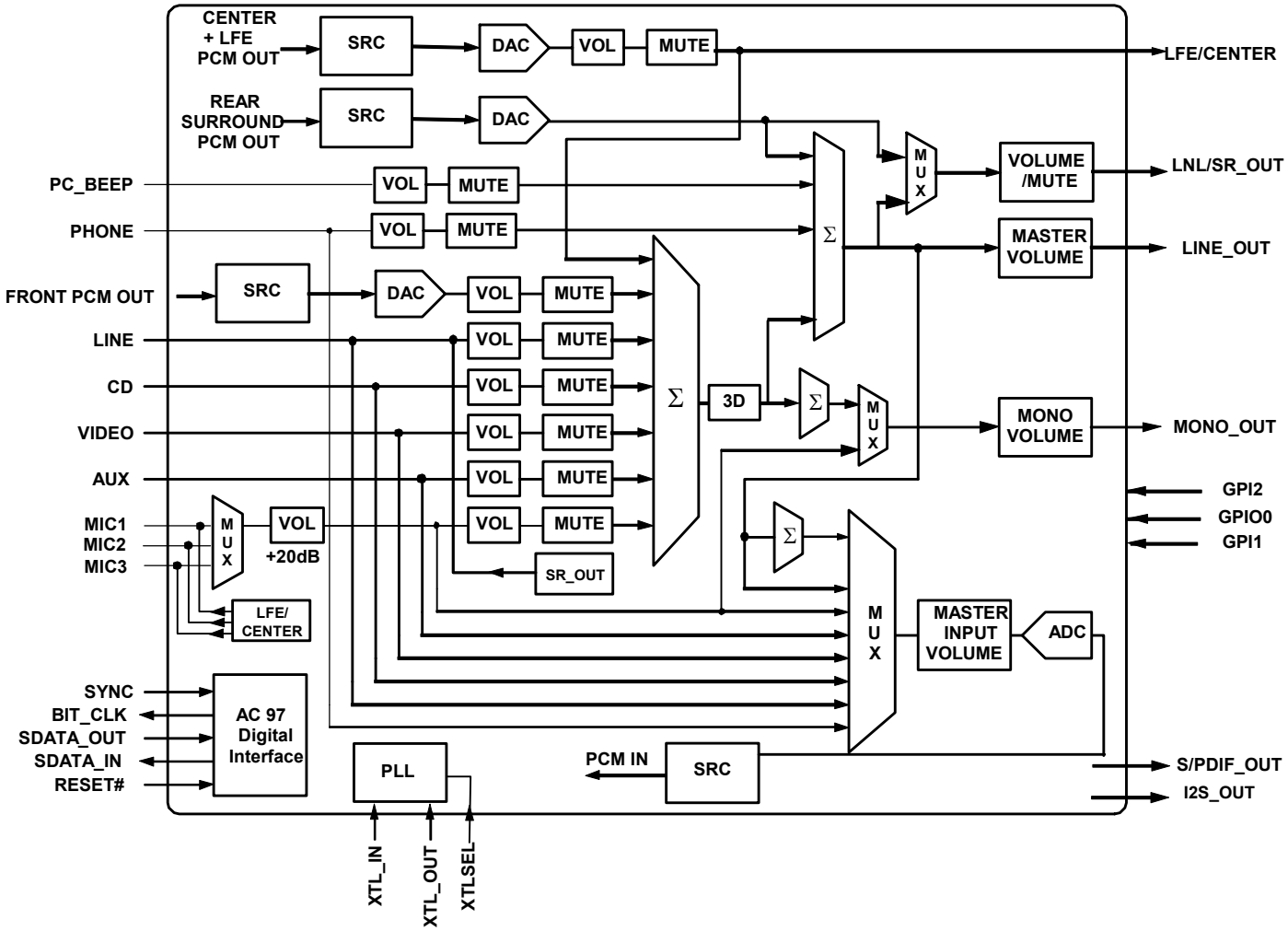


Figure 1. Functional Block Diagram

PINOUTS

Pin Diagram

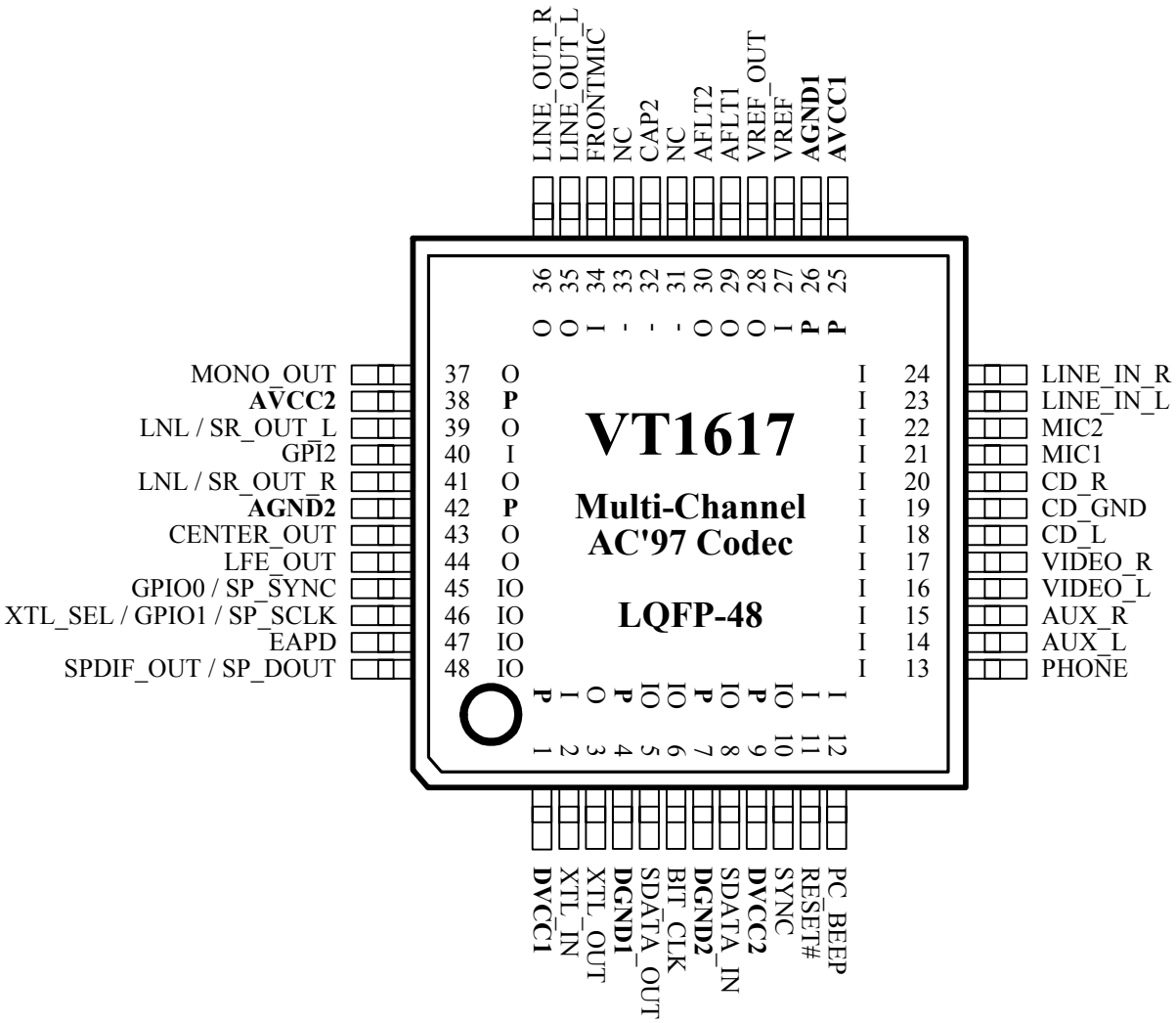


Figure 2. VT1617 Pin Diagram (Top View)

Pin List

Table 1. Pin List (Alphabetical Order)

Pin Name	Pin#	Type	Pin Name	Pin	Type
AFLT1	29	O	LINE_IN_R	24	I
AFLT2	30	O	LINE_OUT_L	35	O
AGND1	**26**	**P**	LINE_OUT_R	36	O
AGND2	**42**	**P**	LNL / SR_OUT_L	39	O
AUX_L	14	I	LNL / SR_OUT_R	41	O
AUX_R	15	I	MIC1	21	I
AVCC1	**25**	**P**	MIC2	22	I
AVCC2	**38**	**P**	MONO_OUT	37	O
BIT_CLK	6	IO	NC	31	-
CAP2	32	-	NC	33	-
CD_GND	19	I	PC_BEEP	12	I
CD_L	18	I	PHONE	13	I
CD_R	20	I	RESET#	11	I
CENTER_OUT	43	O	SDATA_IN	8	IO
DGND1	**4**	**P**	SDATA_OUT	5	IO
DGND2	**7**	**P**	SPDIF_OUT / SP_DOUT	48	IO
DVCC1	**1**	**P**	SYNC	10	IO
DVCC2	**9**	**P**	VIDEO_L	16	I
EAPD	47	IO	VIDEO_R	17	I
FRONTMIC	34	I	VREF	27	I
GPI2	40	I	VREF_OUT	28	O
GPIO0 / SP_SYNC	45	IO	XTL_IN	2	I
LFE_OUT	44	O	XTL_OUT	3	O
LINE_IN_L	23	I	XTL_SEL / GPIO1 / SP_SCLK	46	IO

Note: I = Input, O = Output, OD = Open Drain, P = Power / Ground, A = Analog

Pin Descriptions

Table 2. Pin Descriptions

Pin #	Signal Name	Type	Description
1	**DVCC1**	**P**	Digital Supply Voltage, 3.3V only
2	**XTL_IN**	I	24.576 MHz Crystal
3	**XTL_OUT**	O	24.576 MHz Crystal
4	**DGND1**	**P**	Digital Ground
5	**SDATA_OUT**	IO	AC'97 Serial Data Input Stream
6	**BIT_CLK**	IO	12.288 MHz Serial Data Clock (Internal pull-low)
7	**DGND2**	P	Digital Ground
8	**SDATA_IN**	IO	AC'97 Serial Data Output Stream (Internal pull-low)
9	**DVCC2**	**P**	Digital Supply Voltage, 3.3V only
10	**SYNC**	IO	48 KHz Fixed Rate Sync Pulse
11	**RESET#**	I	AC'97 Master Reset
12	**PC_BEEP**	I	PC Speaker Beep Pass Through
13	**PHONE**	I	Telephony Subsystem Speakerphone
14	**AUX_L**	I	Auxiliary Audio Left Channel
15	**AUX_R**	I	Auxiliary Audio Right Channel
16	**VIDEO_L**	I	Video Audio Left Channel
17	**VIDEO_R**	I	Video Audio Right Channel
18	**CD_L**	I	CD Audio Left Channel
19	**CD_GND**	I	CD Audio Analog Ground
20	**CD_R**	I	CD Audio Right Channel
21	**MIC1**	I	Desktop Microphone
22	**MIC2**	I	Second Microphone
23	**LINE_IN_L**	I	Line In Left Channel
24	**LINE_IN_R**	I	Line In Right Channel
25	**AVCC1**	**P**	Analog Supply Voltage, 5V or 3.3V
26	**AGND1**	**P**	Analog Ground
27	**VREF**	I	Reference Voltage
28	**VREF_OUT**	O	Reference Voltage Output
29	**AFLT1**	O	Left Channel Anti-Aliasing Filter Capacitor
30	**AFLT2**	O	Right Channel Anti-Aliasing Filter Capacitor
31	**NC**	-	No Connect
32	**CAP2**	-	ADC Reference Voltage Capacitor
33	**NC**	-	No Connect
34	**FRONTMIC**	I	Front MIC or 3rd Microphone Input
35	**LINE_OUT_L**	O	Line Out Left Channel
36	**LINE_OUT_R**	O	Line Out Right Channel
37	**MONO_OUT**	O	Mono Output
38	**AVCC2**	**P**	Analog Supply Voltage, 5V or 3.3V
39	**LNL / SR_OUT_L**	O	Alternate Left Line Level out or Rear Channel Left

Table 2. Pin Descriptions (continued)

Pin #	Signal Name	Type	Description
40	**GPI2**	I	General Purpose Input Pin-2
41	**LNL / SR_OUT_R**	O	Alternate Right Line Level out or Rear Channel Right
42	**AGND2**	**P**	Analog Ground
43	**CENTER_OUT**	O	Center Channel Output
44	**LFE_OUT**	O	Low Frequency Effects Output
45	**GPIO0 / SP_SYNC**	IO	GPIO0 or I2S Left/Right clock (Internal pull-high)
46	**XTL_SEL / GPIO1 / SP_SCLK**	IO	Crystal Selection or General Purpose I/O Pin-1 or I^2S serial bit clock (Internal pull-high)
47	**EAPD**	IO	External Power Amplifier Power Down
48	**SPDIF_OUT / SP_DOUT**	IO	PCM / Non-Audio Sony / Philips Digital I/F Output (Internal pull-high). If left floating, S/PDIF not implemented reported on 28h, bit 2 = "0"

Note: I = Input, O = Output, OD = Open Drain, P = Power / Ground, A = Analog

The VT1617 supports +5V or +3.3V analog power supply. For best analog performance use a 5V analog supply. For maximum power savings use 3.3V for both analog and digital sections. You must use 3.3V as the digital supply. The digital I/Os are **NOT** 5V tolerant.

REGISTERS

Register Overview

The following tables summarize all on-chip registers. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 3. Register Map

Index	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset	–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
02h	Stereo Output Volume	Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0
04h	Alt. Line Output Vol.	Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0
06h	Mono Output Volume	Mute	–	–	–	–	–	–	–	–	–	–	MM4	MM3	MM2	MM1	MM0
0Ah	PC Beep Volume	Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–
0Ch	Phone Volume	Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0
0Eh	Mic In Volume	Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0
10h	Line In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
12h	CD In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
14h	Video In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
16h	Aux In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
18h	PCM Out volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
1Ah	Record Select	–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0
1Ch	Record Gain	Mute	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0
20h	General Purpose	–	–	3D	–	DRSS 1	DRSS 0	MIX	MS	LPBK	–	–	–	–	–	–	–
22h	3D Control	–	–	–	–	–	–	–	–	–	–	–	–	DP3	DP2	DP1	DP0
24h	Audio Int. & Paging	I4	I3	I2	I1	I0	–	–	–	–	–	–	–	PG3	PG2	PG1	PG0
26h	Power Down & Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC
28h	Extended Audio ID	ID1	ID0	–	–	REV1	REV0	–	LDAC	SDAC	CDAC	DSA1	DSA0	–	SPDIF	DRA	VRA
2Ah	Ext. Audio Stat/Control	VCFG		PRK	PRJ	PRI	SPCV	–	LDAC	SDAC	CDAC	SSA1	SSA0	–	SPDIF	DRA	VRA
2Ch	PCM Front DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
2Eh	Surround DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
30h	PCM LFE DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
36h	LFE/Center Volume	Mute	–	–	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	–	–	CNT4	CNT3	CNT2	CNT1	CNT0
38h	Surround Volume	Mute	–	–	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	–	–	RSR4	RSR3	RSR2	RSR1	RSR0
3Ah	S/PDIF Control	V	DRS	SSR1	SSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/PCM	PRO
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
5Ah	Vendor Reserved Register	LVL	–	–	LCTF	STF	BPDC	DC	CLE	–	–	–	–	IB1	IB0	–	–
5Ch	Vendor Reserved Register.	VRPD	–	–		LFBO	CBO	SRBO	MBO	DMIX	HPT	HPE	–	–	–	–	–
60h	Codec Class/Rev	–	–	–	CL4	CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
6Ch	DAC Slot Mapping	FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	–	–	–	–
6Eh	ADC Slot Mapping	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MV
76h	Miscellaneous	–	–	–	–	–	–	SDRSS	–	DRA_OFF	CD2SP	–	–	SP96	6CH_DRA	EN_DRA	I2SE
78h	GPIO Control	GSI	GOS	–	–	–	GW2	GW1	GW0	–	GP2	GP1	GP0	–	–	GC1	GC0
7Ah	GPIO Status	SM51SW	SM51EN	–	–	–	–	GOC1	GOC0	–	GIS2	GIS1	GIS0	–	GI2	GI1	GI0
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Register Descriptions

Reset Register (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6D50h

The Reset register is used to configure the hardware to a known state or to read the ID code of the part. A code was assigned to VIA Technologies (27 = 11011h) for 3D Stereo Enhancement reflected in SE[4:0]. ID8 and ID6 are set to 1b to report that the ADC and DAC are 20-bit resolution respectively. The VT1617 supports an alternate line level out with independent volume control as reflected by ID4=1b. However, since pins 39 and 41 are shared with the Surround DAC outputs, register 5Ah, bit 15, LVL has to be set to "1". Writing data to this register will set all the mixer registers to their default values. For description of the bits set to 0b, refer to AC'97 Rev. 2.3 spec.

Stereo Output Control Register (Index 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0	8000h

Mute **Stereo Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

ML[4:0] **Master Output (Left Channel) Volume Control**

These five bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

MR[4:0] **Master Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

Alternate Line Output Control Register (Index 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	ML4	ML3	ML2	ML1	ML0	–	–	–	MR4	MR3	MR2	MR1	MR0	8000h

Note: Pins 39 and 41 are shared with the Surround DAC outputs. LVL, register 5Ah, bit 15, has to be set to "1"

Mute **Stereo Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

ML[4:0] **Alternate Line Output (Left Channel) Volume Control**

These six bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

MR[4:0] **Alternate Line Output (Right Channel) Volume Control**

These five bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

Mono Output Control Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	MM4	MM3	MM2	MM1	MM0	8000h

Mute **Mono Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

MM[4:0] **Mono Output Volume Control**

These five bits select the level of attenuation applied to the Mono Output signal. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

Table 4. Stereo and Mono Output Attenuation

	M4	M3	M2	M1	M0	Level (dB)
0	0	0	0	0	0	0.0
1	0	0	0	0	1	-1.5
2	0	0	0	1	0	-3.0
3	0	0	0	1	1	-4.5
4	0	0	1	0	0	-6.0
5	0	0	1	0	1	-7.5
..	..	..	..	..	..	..
..	..	..	..	..	..	..
28	1	1	1	0	0	-42.0
29	1	1	1	0	1	-43.5
30	1	1	1	1	0	-45.0
31	1	1	1	1	1	-46.5

PC Beep Input Volume Control Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–	8000h

Mute **PC Beep Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

PV[3:0] **PC Beep Input Volume Control**

These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[3:0] = 0h. Even though the default of the input volume control is mute, as long as RESET# is active, PC Beep will be passively routed to the line outputs.

Phone Input Volume Control Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Phone Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GN[4:0] **Phone Input Volume Control**

These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

Mic Input Volume Control Register (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Mic Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

20dB **Mic Boost Control**

"1" : Fixed 20dB gain enabled

"0" : Fixed 20dB gain disabled

GN[4:0] **Mic Input Volume Control**

These five bits select the gain applied to the Mic Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

Line Input Control Register (Index 10h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Line Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

CD Input Control Register (Index 12h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **CD Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

Video Input Control Register (Index 14h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Video Input Mute Control**

"1" : Mute enabled "0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

Auxiliary Input Control Register (Index 16h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Auxiliary Input Mute Control**

"1" : Mute enabled "0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the Left channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the Right channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

PCM Output Control Register (Index 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **PCM Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 5** on page 16 for details.

Table 5. Programmable Mixer Input Gain Levels

	G4	G3	G2	G1	G0	Level (dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

Record Select Register (Index 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0	0000h

SL[2:0] **Record Source Select (Left Channel)**

These bits determine the record source for the left channel.

SL2	SL1	SL0	Left Record Source
0	0	0	Mic
0	0	1	CD (L)
0	1	0	Video In (L)
0	1	1	Aux In (L)
1	0	0	Line In (L)
1	0	1	Stereo Mix (L)
1	1	0	Mono Mix
1	1	1	Phone

SR[2:0] **Record Source Select (Right Channel)**

These bits determine the record source for the right channel.

SR2	SR1	SR0	Right Record Source
0	0	0	Mic
0	0	1	CD (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

Record Gain Control Register (Index 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0	8000h

Mute **Record Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[3:0] **Record Gain Control (Left Channel)**

These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.

GR[3:0] **Record Gain Control (Right Channel)**

These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GR[3:0] = 0h.

General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	3D	–	DRSS1	DRSS0	MIX	MS	LPBK	–	–	–	–	–	–	–	0000h

3D **3D Stereo Enhancement**

"1" : Enable 3D

"0" : Disable 3D

DRSS[1:0] **Double Rate Slot Select**

"00" : PCM L, R, C n+1 data is on Slots 10-12 (default)

"01" : PCM L, R n+1 data is on slots 7, 8

Others: Reserved

MIX **Mono Output Mode**

"1" : Mic Output

"0" : Mono mix output

MS **Microphone Select (See Table below)**

Table 6. Mixer Table

Controller Bit			MICIN		I/O				
SM51	SM51SW	SMIC	20XL	20XR	MIC1	MIC2	MIC3	LL	LR
0	0	0	MIC1	MIC1	MIC1	-	-	LL	LR
0	0	1	MIC1	MIC3	MIC1	-	MIC3	LL	LR
0	1	0	MIC2	MIC2	-	MIC2	-	LL	LR
0	1	1	MIC1	MIC2	MIC1	MIC2	-	LL	LR
1	0	0	MIC3	MIC3	CEN	LFE	MIC3	SURL	SURR
1	0	1	MIC3	MIC3	CENT	LFE	MIC3	LL	LR
1	1	0	MIC1	MIC1	Mic1		LFE	SURL	SURR
1	1	1	MIC1	MIC2	MIC1	MIC2-	LFE	SURL	SURR

LPBK **Loopback Mode**

"1" : DAC/ADC Loopback enabled

"0" : DAC/ADC Loopback disabled

3D Control Register (Index 22h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	–	–	–	–	–	–	DP3	DP2	DP1	DP0	0000h

DP[3:0] **3D Depth Control**

These four bits control the linear depth control of the 3D stereo enhancement built into the codec. The gain is programmable from 0% to 100% in 6.67% increments, providing a total of 16 programmable levels. The default value corresponds to no stereo enhancement.

Table 7. 3D Depth Control

	DP3	DP2	DP1	DP0	Level (%)
0	0	0	0	0	0.0
1	0	0	0	1	6.67
2	0	0	1	0	13.33
3	0	0	1	1	20
4	0	1	0	0	26.67
5	0	1	0	1	33.33
..	..	..	..	..	..
..	..	..	..	..	..
12	1	1	0	0	80
13	1	1	0	1	86.67
14	1	1	1	0	93.33
15	1	1	1	1	100

Audio Interrupt and Paging Mechanism Register (Index 24h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC	0000h

Bit	Default	Function
I4	0	Interrupt Status (R/W) 0 - Interrupt is clear 1 - Interrupt was generated Interrupt event is cleared by writing a 1 to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the AC link will follow this bit change when interrupt enable (I0) is un-masked. If this bit is set, one or both of I3 or I2 must be set to indicate the interrupt cause.
I[3:2]	00	Interrupt Cause (RO) I [2]= 0 - Reserved I [3]= 0 - GPIO status change did not cause interrupt (default) 1 - GPIO status change caused interrupt. These bits will indicate the cause(s) of an interrupt. This information should be used to service the correct interrupting event(s). If the Interrupt Status (bit I4) is set, one or both of these bits must be set to indicate the interrupt cause. Hardware must reset these bits back to zero when the Interrupt Status bit is cleared.
I1	0	Reserved
I0	0	Interrupt Enable (RW) 0 - Interrupt generation is masked 1 - Interrupt generation is un-masked S/W should Not un-mask the interrupt unless ensured by the AC '97 controller that no conflict is possible with modem slot 12- GPI functionality. AC '97 2.2 compliant controllers will not likely support audio codec interrupt infrastructure.
PG[3:0]	0h	Page Selector (RW): 0h - Vendor Specific 1h – Page ID 01(see correspondent definition register 60h-6Fh) 2h-Fh – Reserved Pages This register is used to select a descriptor of 16 word pages between registers 60h to 6Fh. A value of 0h is used to select vendor specific space to maintain compatibility With AC '97 2.2 vendor specific registers. System software can determine implemented pages by writing the page number and reading the value back. If the value read back does not match the value written, the page is not implemented. All implemented pages must be in consecutive. (i.e., page 2h cannot be implemented without page 1h)

Power Down and Status Register (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC	0000h

EAPD **Enable Amplifier Power Down**

"1" : Powerdown External Power Amplifier

"0" : External Power Amplifier active

The signal polarity at pin 47, EAPD is identical to bit description.

PR[6:0] **Power Down Mode Bits**

These read/write bits are used to control the power down states of the VT1617. Each power down function bit is enabled by setting the respective bit high. Particularly, PR5 has no effect unless PR0, PR1 and PR4 are all set to "1". This implies that the codec can be woken up by a warm reset, because warm reset clears PR4, which in turn disables the function of PR5. The register bit, however will not be cleared by a warm reset. The power down modes controlled by each bit is described in the table below:

Bit	Function
PR0	ADC and Mux Powerdown
PR1	DAC Powerdown
PR2	Mixer Powerdown (VREF on)
PR3	Mixer Powerdown (VREF off)
PR4	AC Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disabled
PR6	Alternate Line Out Powerdown

REF,ANL,ADC,DAC **Status (READ Only) bits**

These bits are used to monitor the readiness of some sections of the VT1617. Reading a "1" from any of these bits would be an indication of a "ready" state.

Bit	Status Bit
REF	VREF at nominal level
ANL	Mixer, Mux and Volume Controls ready
DAC	DAC ready to accept data
ADC	ADC ready to transmit data

Extended Audio ID Register (Index 28h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
ID1	ID0	–	–	REV1	REV0	–	LDAC	SDAC	CDAC	DSA1	DSA0	–	SPDIF	DRA	VRA	09Cxh

The Extended Audio ID is a read only register that indicates the capabilities of the VT1617.

ID[1:0] **(See Table below)**

One primary and an additional codec may be supported as an option. Since the VT1617 codec has all six outputs implemented, the ID pin setting affects only the BIT_CLK direction and the register decoding. BIT_CLK output the power-up default. Setting the codec besides default changes BIT_CLK to input mode. As indicated by D9, AMAP=0, there is no need to change slot mappings.

Table 8. Multiple Code Mode Status Bits

ID1	ID0	Codec Mode
0	0	Primary Codec (default)
0	1	Secondary Codec
1	0	Invalid
1	1	Invalid

Note: The state of the ID pins is reported in reverse polarity on register 28h, bits D15 and D14. If you use this table to configure the codec via pins 45 and 46, use the inverse values. BIT_CLK is an output for the primary codec and an input pin for the controller and secondary codecs. ID[1:0] pins with internal pull-up resistors defaults codec as primary codec.

REV[1:0] **AC'97 Revision ID**

REV[1:0]=10 indicates Codec is AC '97 revision 2.3 compliant.

xDAC **Multi-channel Output Capabilities**

"1": LDAC, SDAC, CDAC report to the querying host that the codec has all six outputs implemented.

DSA[1:0] **DAC Slot Assignment(See Table below)**

DSA[1:0] are read/write bits that control optional DAC Slot Assignment.

DSA1, DSA0	DACs 1,2	DACs 3,4	DACs 5,6
00	slots 3&4	slots 7&8	slots 6&9
01	7&8	6&9	10&11
10	6&9	10&11	3&4
11	10&11	3&4	7&8

SPDIF **Sony/Philips Digital Audio Interface**

"1" : Feature implemented in compliance to "S/PDIF Output for AC '97, Rev 1.0"

"0" : Indicates that SPDIF_OUT pin 48 is left floating or pulled-high. It reflects the lack of external S/PDIF application circuitry.

DRA **Double Rate PCM Audio**

"1" : optional Double-Rate PCM Audio output is supported

VRA **Variable Sampling Rate PCM Audio**

"1" : Feature implemented in compliance to AC '97 2.2 Appendix A

Extended Audio Status/Control Register (Index 2Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
VCFG	–	PRK	PRJ	PRI	SPCV	–	LDAC	SDAC	CDAC	SSA1	SSA0	–	SPDIF	DRA	VRA	3860h

VCFG **S/PDIF Valid Configuration**

determines S/PDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF "Validity" flag, which is bit 28 transmitted in each S/PDIF sub-frame.

PRx **Multi-channel Output Control**

All three bits, PRK, PRJ, PRI behave similarly. When set to "0", the respective DAC(s) is (are) turned on. PRK is for LFE, PRJ for Surround (Rear pair), PRI for Center channel.

SPCV **S/PDIF Configuration Valid (Read Only)**

"0" : S/PDIF configuration (SSA, SSR, DAC rate, DRS) invalid (not supported)

"1" : S/PDIF configuration (SSA, SSR, DAC rate, DRS) valid (supported)

xDAC **Multi-channel Output Status (Read Only)**

These read only bits, LDAC, SDAC, CDAC behave similarly. When they report "1", the respective DAC(s), LFE, Surround and Center is (are) ready.

SSA[1:0] **S/PDIF Slot Assignment**

These bits determine the S/PDIF data source from AC-link slot selection when SPDIF_OUT, pin 48 is low during reset (pulled low by external application circuit). If the S/PDIF application circuit is not implemented, these bits will return only 0. The default state reflects the pervasive design feature of common AC'97 digital controllers supporting slots 3 & 4. Slots 10 & 11 are expected to be used in the future to support concurrent 6 channels analog and 2 channel digital audio (compressed or LPCM).

SSA1	SSA0	S/PDIF Source Data
0	0	AC-link slots 3 & 4 (front stereo pair, power-up default)
0	1	AC-link slots 7 & 8 (surround pair)
1	0	AC-link slots 6 & 9 (LFE & Center pair)
1	1	AC-link slots 10 &11

SPDIF **Sony/Philips Digital Audio Interface Enable/Disable**

"1" : Set this bit to turn on the S/PDIF transmitter.

"0" : The S/PDIF transmitter is off by default.

DRA **Double Rate Mode control**

"1" : Enable Double-Rate Audio mode in which data from PCM L and PCM R in output slots 3 and 4 is used in conjunction with PCM L (n+1) and PCM R (n+1) data, to provide DAC streams at twice the sample rate designated by the PCM Front Sample Rate Control Register.

VRA **Variable Sampling Rate Mode control**

"1" : Enable VSR

"0" : Fixed 48 KHz sampling rate

PCM Front and Center DAC Sample Rate Register (Index 2Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **Main stereo + Center or all DAC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h). This register controls all six DAC output rate providing a sample accurate synchronization among the channels. Registers 2Eh and 30h are read/writable but have no control over the Surround and LFE channels. They reflect 2Ch when read back.

PCM Surround DAC Sample Rate Register (Index 2Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **Surround DAC Sample Rate (in Hz)**

16-bit unsigned alias value of 2Ch representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h). This register has no physical control over the Surround pair DACs sampling rate.

PCM LFE DAC Sample Rate Register (Index 30h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **LFE DAC Sample Rate (in Hz)**

16-bit unsigned alias value of 2Ch representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h). This register has no physical control over the LFE DAC's sampling rate.

PCM ADC Sample Rate Register (Index 32h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

SR[15:0] **ADC Sample Rate (in Hz)**

16-bit unsigned value representing the sample rate in 1Hz resolution. The default value is 48 KHz (48000 = BB80h).

LFE and Center Channels Output Volume Control Register (Index 36h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	LFE4	LFE3	LFE2	LFE1	LFE0	Mute	–	–	CNT4	CNT3	CNT2	CNT1	CNT0	8080h

Mute **Individual Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

LFE[4:0] **LFE Output Volume Control**

These five bits select the level of attenuation applied to the Low Frequency Effect channel. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

CNT[4:0] **Center Channel Output Volume Control**

These five bits select the level of attenuation applied to the Center channel. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

Surround Channels Output Volume Control Register (Index 38h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	LSR4	LSR3	LSR2	LSR1	LSR0	Mute	–	–	RSR4	RSR3	RSR2	RSR1	RSR0	8080h

Note: Pins 39 and 41 are shared with the Alternate Line Level Out, main stereo DAC outputs. LVL, register 5Ah, bit 15, has to be set to "0" for this register to be effective on the same volume control block.

Mute **Individual Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

LSR[4:0] **Left Surround (Rear) Channel Output Volume Control**

These five bits select the level of attenuation applied to the Left Surround channel. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

RSR[4:0] **Right Surround (Rear) Channel Output Volume Control**

These five bits select the level of attenuation applied to the Right Surround channel. The level of attenuation is programmable from 0dB to -46.5dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 4** on page 11 for details.

S/PDIF Control Register (Index 3Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
V	DRS	SSR1	SSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/PCM	PRO	x000h

This read/write register controls the S/PDIF functionality when SPDIF bit at 28h_2 reports S/PDIF is implemented. It will return 0000h when SPDIF_OUT, pin 48 left floating or pulled high. If S/PDIF is implemented for the final product, it will read 2000h at power-up. The register manages the bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should only be written when the S/PDIF transmitter is disabled (SPDIF bit at 2Ah_2 is "0"). This ensures that control and status information start up correctly at the beginning of S/PDIF transmission.

V **Validity**

This bit affects the "Validity flag", bit<28> transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the VCFG bit in the Extended Audio Status and Control register. The behavior of the transmitter is defined in the definition of the Extended Audio Status and Control Register (Index 2Ah)

DRS **Double Rate S/PDIF**

When DRS is enabled "1" and SPSA is configured {"01", "10", or "11"} the S/PDIF transmitter uses AC-link slots 3&4 + {7&8, 6&9, or 10&11} to supply data at Fs = 64, 88.2 or 96 kHz.

SSR[1:0] **S/PDIF Sample Rate**

These bits declare the available S/PDIF transmitter clock rate (64*fs).

SSR1	SSR0	S/PDIF Sample Rate
0	0	Not Available
0	1	Reserved
1	0	48 KHz (default)
1	1	Not Available

L **Generation Level**

Programmed according to IEC standards.

CC[6:0] **Category Code**

Programmed according to IEC standards.

PRE **Preemphasis**

"1" : Indicates filter preemphasis is 50/15µs.

"0" : Default is no Preemphasis.

COPY **Copyright**

"1" : Indicates copyright is asserted.

"0" : Copyright is not asserted (default).

/PCM **Non-Audio Samples**

"1" : Set this bit for transmitting non-PCM audio samples such as AC-3.

"0" : Indicates samples are linear PCM suitable for direct conversion to audio playback.

PRO **Professional**

"1" : Set Professional mode. Set this bit in conjunction with /PCM bit (above) for AC-3.

"0" : Indicates Consumer mode (default).

Vendor Reserved Register (Index 5Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
LVL	Res.	Res.	LCTF	STF	BPDC	DC	CLE	Res.	Res.	Res.	Res.	IB1	IB0	Res.	Res.	8200h

Res. **Test Mode Bits**

These read/write bits are used for testing the digital modes of the audio codec. Do not access them during Normal operation.

LVL **Alternate Line Level Out to Surround Out**

The VT1617 powers up with pins 39 and 41 assigned to the Front channel DACs as described in the AC97 Revision 2.2 specification. When this bit is to "0", the output pins get assigned to the Rear stereo DAC pair with an independent volume control.

LCTF **Downmix LFE and Center DAC outputs to the Front channels**

The VT1617 is capable of downmixing the LFE and the Center channel outputs to the Line_Out pins using internal hardware. Without processing overhead, it is possible to listen to all the channels without loss of audio cues. The relative SPL (Sound Pressure Level) for these channels are retained as meant by the digital audio content mastering engineer. This is ideal for 4-channel applications.

STF **Downmix Surround DAC outputs to the Front channels**

The VT1617 is capable of downmixing the Rear channel outputs to the Line_Out pins using internal hardware besides the LFE and the Center. This is useful when multichannel material needs to be played back on a stereo end point like headphones. Without processing overhead, it is possible to listen to all the channels without loss of audio cues. The relative SPL (Sound Pressure Level) for these channels are retained as meant by the digital audio content mastering engineer. This is ideal for 2-channel applications when LCTF and STF are both activated at the same time.

BPDC **ADC DC-offset Removal Control**

The default setting of "0" ensures that the circuit is disabled at power up. When set to "1", the DC- offset cancellation circuit will be enabled. This helps to maximize recording quality by removing white noise.

DC **DC-offset Removal Capability**

This read only bit indicates that the codec incorporates DC-offset removal hardware.

CLE **Center/LFE DAC Data Exchange**

"1" : Exchange PCM data in Center DAC and LFE DAC

IB[1:0] **Analog Current Setting Bits**

Normally these bits should be left at default when analog operating at 5V supply. The four possible settings adjust the power consumption of the analog section. The power-up default 00b sets the codec for the best overall analog performance at 5V. At 3.3V analog supply, 10b should be set for the lowest power instead of default 00b. This mode is desirable for system designs with limited power budget such as battery operated portable devices. Setting to 11b puts the codec to its best A- A mixer performance overall.

IB1	IB0	Analog Current Setting
0	0	Normal (1X)
0	1	Reduced (4/5X)
1	0	Power Miser (2/3X)
1	1	Enhanced (4/3X)

Vendor Reserved Register (Index 5Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
VRPD	Res.	Res.	Res.	LFBO	CBO	SRBO	MBO	DMIX	HPT	HPE	Res.	Res.	Res.	Res.	Res.	0000h

VRPD **Vrefout power down**

"1" : Vrefout power down

xBO **Output Channel 1.5dB Boosting Control**

"1" : the respective DAC channel, LFE, Center and Surround has 1.5dB boosting

DMIX **FrontMic and Mic2 downmix select**

"1" : downmix to L/R channel

"0" : FrontMic in Left channel, Mic2 in Right channel

HPT **Headphone Amplifier Thermal Protection Shutdown**

This read only bit gets automatically set to '1' and reports when the thermal protection threshold has been exceeded. It will be reset to '0' when the offending high temperature condition is removed and the normal operation state is re-entered.

HPE **Headphone Amplifier Temperature Sensing Control**

This bit when set to '1' disables the built-in thermal sensor for protection of the headphone amplifier. Default power-up state '0', thermal protection is on. If the thermal ceiling is exceeded, the headphone output will be shut off.

Res. **Test Mode Bits**

These read/write bits are used for testing the digital modes of the audio codec. Do not access them during Normal operation.

Codec Class/Rev Register (Index 60h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	CL4	CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0	0000h

CL[4:0] **Codec Compatibility Class (RO)**

00h – Field not implemented

01h-1Fh – Vendor specific compatibility class code

RV[7:0] **Revision ID(RO)**

DAC Slot Mapping Register (Index 6Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
FD3	FD2	FD1	FD0	SD3	SD2	SD1	SD0	CLD3	CLD2	CLD1	CLD0	–	–	–	–	3760h

FD[3:0] **Front Channel DAC Slot Mapping Control**

Control the mapping of the 1st DAC pair (generally the front speakers and headphone), which defaults to slots 3 and 4.

SD[3:0] **Surround Channel DAC Slot Mapping Control**

Control the mapping of the 2nd DAC pair (generally the surround speakers), which defaults to slots 7 and 8

CLD[3:0] **Center/LFE Channel DAC Slot Mapping Control**

Control the mapping of the 3rd DAC pair (generally the center and LFE speakers), which defaults to slots 6 and 9.

ADC Slot Mapping Register (Index 6Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	MV	0000h

MV **Mapping Valid**

Indicates that the values programmed into page offsets 6Ch and 6Eh are valid.

Miscellaneous Register (Index 76h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	SDRSS	–	DRA_OFF	CD2SP	–	–	SP96	6CH_DRA	EN_DRA	I2SE	0000h

SDRSS **Special Double Rate Slot Select**

"1" : PCM L, R, C n+1 data is on Slots 7-9 (This is non-AC97 mode)

"0" : DRA slot select decided by REG20.DRSS

DRA_OFF **Disable 6 channels double rate playback. (Read Only)**

This bit would be set to 1 if 1024 consecutive samples on SDOUT1 are 0 or 20'hffffff

CD2SP **CD input to S/PDIF out**

"1" : S/PDIF output data comes from ADC

"0" : S/PDIF output data comes from SDATA_OUT

SP96 **Enable S/PDIF 96K mode**

"1" : Slot 10 and Slot 11 of SDATA_OUT1, the slave pin to SDATA_OUT, will carry the N+1 samples of the S/PDIF data.

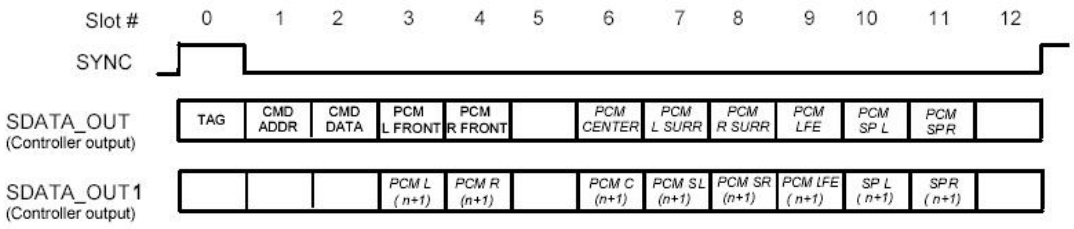
6CH_DRA **Enable 6 channels double rate playback mode**

"1" : Slot 3, Slot 4, Slot 6, Slot 7, Slot 8 and Slot 9 of SDATA_OUT1, the slave pin to SDATA_OUT, will carry the N+1 samples of the audio PCM.

EN_DRA **Double rate playback (Read Only)**

"1" : Feature implemented.

"0" : Indicates that SDATA_OUT1 is pulled-high or floating. It reflects the lack of SDATA_OUT1 circuit



I2SE **I2S Enable**

"1" : Pin 45, Pin 46 and Pin 48 will output SP_SYNC, SP_SCLK and SP_DOUT.

GPIO Control Register (Index 78h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
GSI	GOS	–	–	–	GW2	GW1	GW0	–	GP2	GP1	GP0	–	–	GC1	GC0	0070h

GSI **GPIO Interrupt Status Indication in SDATA_IN**

"0" : The status of GPIO and its valid tag are not indicated in SDATA_IN.

"1" : The status of GPIO and its valid tag are indicated in SDATA_IN.

GOS **GPIO output select**

"0" : GPIO output is controlled by Reg7A[5:4].

"1" : GPIO output is controlled by SDATA_OUT Slot12 bit5 & bit4.

GW[2:0] **GPIO Pin interrupt enable when GPIO is used as input**

"0" : Disable

"1" : Enable

GP[2:0] **GPIO Interrupt Polarity**

"0" : Low to High transition

"1" : High to Low transition

GC[1:0] **GPIO Pin Configuration**

"0" : GPIO pin is used as input

"1" : GPIO pin is used as output

GPIO Status Register (Index 7Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SM51SW	SM51EN	–	–	–	–	GOC1	GOC0	–	GIS2	GIS1	GIS0	–	GI2	GI1	GI0	0000h

SM51SW **Smart 5.1 feature. (See Mixer Table)**

SM51EN **Smart 5.1 feature. (See Mixer Table)**

GOC[1:0] **GPIO Output Control**

"0" : Drive GPIO low

"1" : Drive GPIO high

GIS[2:0] **GPIO Input Status (When GPIO is used as input)**

"0" : GPIO[n] is driven low

"1" : GPIO[n] is driven high

GI[2:0] **GPIO Interrupt Status (When GPIO is used as input)**

"0" : No GPIO interrupt

"1" : GPIO interrupt

Write 1 to clear this status bit.

Vendor Identification Register (Index 7Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5649h

The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the VT1617. The Vendor ID Code (in ASCII format) is equal to "VIA", where:

F[7:0] **Upper Byte (Index 7Ch) D[15:8] = V**

S[7:0] **Lower Byte (Index 7Ch) D[7:0] = I**

T[15:8] **Upper Byte (Index 7Eh) D[15:8] = A**

Revision Identification Register (Index 7Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4170h

The upper byte of this register is used in conjunction with index register 7Ch to make up the Vendor ID code for the VT1617. The lower byte identifies VT1617 and its revision code.

T[15:8] **See description in Vendor Identification Register.**

REV[7:0] **Revision ID**

"70" : VT1617 identification and revision number

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
T_{STG}	Storage Temperature	–55		125	ºC
T_C	Case Operating Temperature	0		85	ºC
V_{IN}	Input Voltage (All Digital Pins)	GND – 0.5		VCC + 0.5	V
V_{ESD}	Electrostatic Discharge (Human Body)			2	KV
T_{VPS}	Vapor Phase Soldering (One Minute)			220	ºC

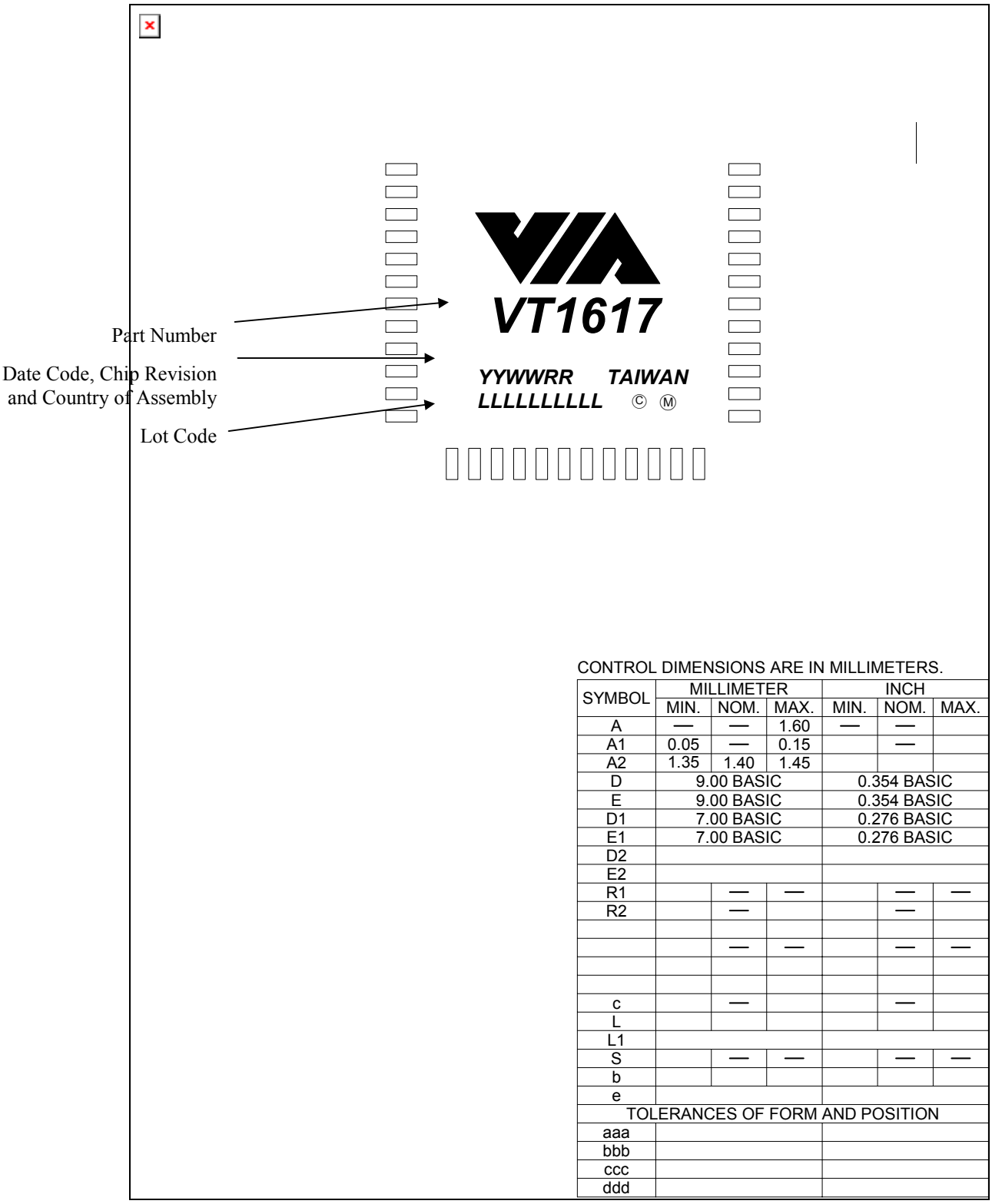
Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33	Digital Power Supplies (DVCC)	3.135	3.3	3.465	V
VCC5	Analog Power Supplies (AVCC), preferred	4.75	5	5.25	V
VCC5	Analog Power Supplies (AVCC), for low-power apps	3.135	3.3	3.465	V

DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	-0.3		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–		0.3 V_{CC}	V
V_{IH}	Input High Voltage	0.7 V_{CC}		–	V
V_{OL}	Output Low Voltage	–		0.4	V
V_{OH}	Output High Voltage	2.4		–	V

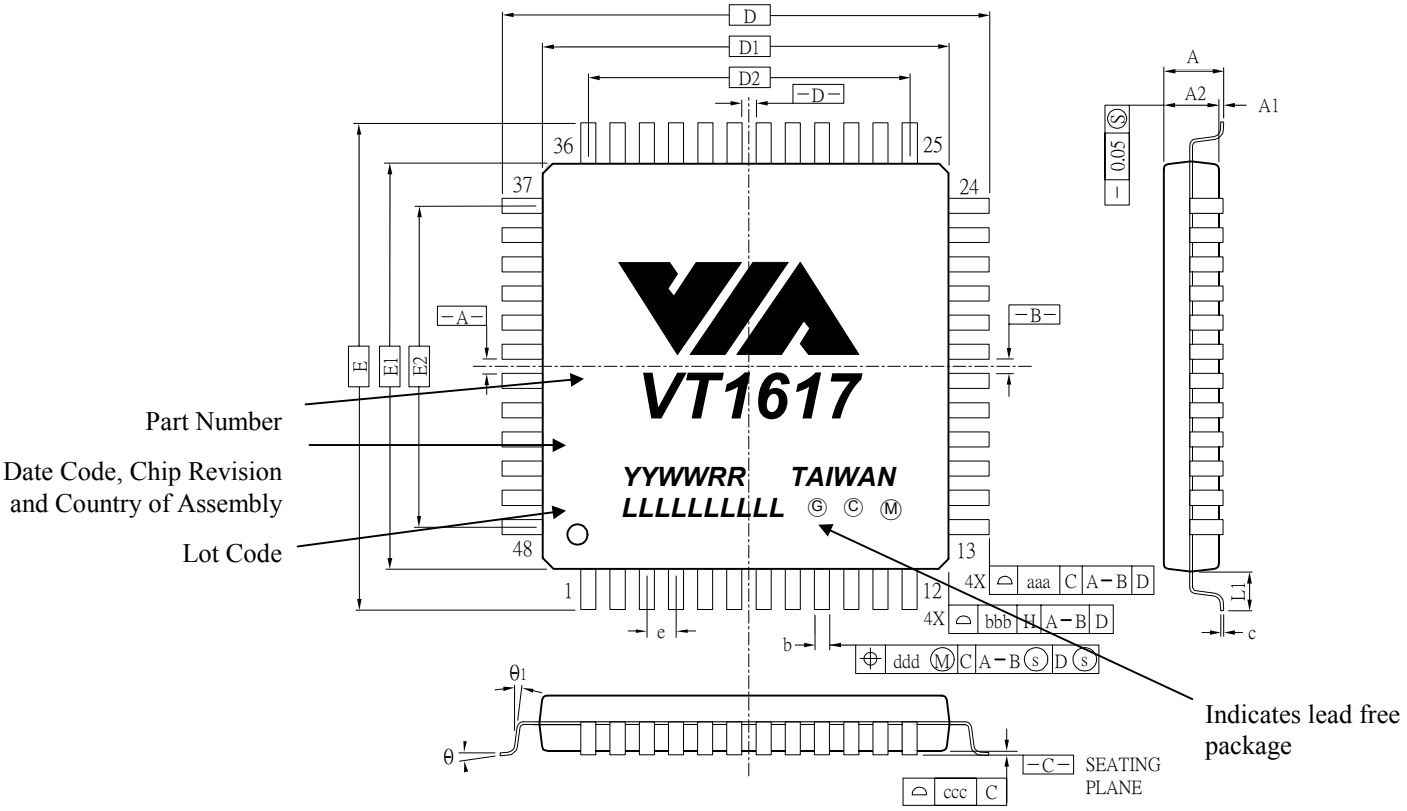
PACKAGE MECHANICAL SPECIFICATIONS



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	
A1	0.05	—	0.15		—	
A2	1.35	1.40	1.45			
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2						
E2						
R1		—	—		—	—
R2		—			—	
		—	—		—	—
c		—			—	
L						
L1						
S		—	—		—	—
b						
e						
TOLERANCES OF FORM AND POSITION						
aaa						
bbb						
ccc						
ddd						

Figure 3. Mechanical Specification – 48-Pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 4. Mechanical Specification for Lead Free – 48-Pin LQFP